CONTENT ADDRESSABLE MEMORY (CAM) DEVICES THAT SUPPORT DISTRIBUTED CAM CONTROL AND METHODS OF OPERATING SAME

Abstract of the Disclosure

Content addressable memory (CAM) devices include CAM logic that is configured to pass an instruction received at an instruction input port to an instruction output port without inspection or alteration. This enables the CAM devices to be operated as equivalent devices within a cascaded chain of CAM devices that collectively form multiple databases within a lookup engine having distributed CAM control. This CAM logic may include an input instruction register that is configured to latch the instruction received at the instruction input port and an output instruction register that is configured to latch the instruction received from the input instruction register. This CAM logic may also include an instruction FIFO that is configured to buffer instructions received from the input instruction register. A method of performing a learn operation in a cascaded chain of CAM devices may include writing a search key associated with a database into a selected one of the cascaded chain of CAM devices, in response to evaluating whether an NFA table in the selected one of the cascaded chain of CAM devices has a valid NFA address for the search key. Then, following the write operation, an operation may be performed to search each of the CAM devices in the cascaded chain to identify an address of a highest priority invalid entry in a CAM device that retains at least a portion of the database.

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